Amended Claims With Mark-ups to Show Changes Made

15. (Amended) A method for fabricating a nonvolatile ferroelectic memory device, the method comprising:

defining a first active region and a second active region on a semiconductor substrate;

forming first split wordline across the first active region and a second split wordline across the second active region;

forming first and second source and drain regions in the first and second active regions, respectively, wherein the source and drain regions are at opposite sides of the first and second split wordlines;

forming first plugs coupled to the first and second drain regions through a contact hole;

forming second plugs coupled to the first and second source regions through the [contract] contact hole;

respectively forming first electrodes of first and second ferroelectric capacitors over the second and first split wordlines;

forming ferroelectric layers on the first electrodes;

respectively forming [island shaped] second electrodes of the first and second ferroelectric capacitors on surfaces of the first and second ferroelectric layers;

respectively forming first and second conductive layers that couple the second plugs with the second electrodes of the first and second ferroelectric capacitors; and

forming first and second bitlines across the first and second split wordlines, wherein the first and second bitlines are coupled to the first and second drain regions through the first plugs.

Clean Set of Amended Claims

15. (Amended) A method for fabricating a nonvolatile ferroelectic memory device, the method comprising:

defining a first active region and a second active region on a semiconductor substrate;

forming first split wordline across the first active region and a second split wordline across the second active region;

forming first and second source and drain regions in the first and second active regions, respectively, wherein the source and drain regions are at opposite sides of the first and second split wordlines;

forming first plugs coupled to the first and second drain regions through a contact hole;

forming second plugs coupled to the first and second source regions through the contact hole;

respectively forming first electrodes of first and second ferroelectric capacitors over the second and first split wordlines;

forming ferroelectric layers on the first electrodes;

respectively forming second electrodes of the first and second ferroelectric capacitors on surfaces of the ~~first and second~~ ferroelectric layers;

respectively forming first and second conductive layers that couple the second plugs with the second electrodes of the first and second ferroelectric capacitors; and

forming first and second bitlines across the first and second split wordlines, wherein the first and second bitlines are coupled to the first and second drain regions through the first plugs.

C. Please add new claims 25-41 as follows:

25. (New) The method of claim 15, wherein the second electrodes of the first and second ferroelectric capacitors are island shaped, and wherein the first and second active regions are asymmetrically positioned.

26. (New) The method of claim 15, wherein the first conductive layer directly connects the second electrode of the first ferroelectric capacitor with the second plug coupled to the first source region of the first active region, and wherein the second conductive layer directly couples the second electrode of the second ferroelectric capacitor with the second plug coupled to the first source region of the second active region.

27. (New) The method of claim 15, comprising:

forming a cell array having a matrix form of split wordline pairs crossing bitlines;

forming a wordline driver coupled to the wordlines;

forming a decoder coupled to the bitlines; and

forming an output unit coupled to the bitlines, wherein corresponding first and second split wordlines form split wordline pairs.

28. (New) A method for fabricating a device, the method comprising:

forming first and second split wordlines on a substrate extending along a first direction separated by a prescribed interval;

forming first and second impurity regions respectively along opposite sides of each of the first and second split wordlines;

respectively forming first and second capacitors over the second and first split wordlines;

respectively forming first and second conductive layers that respectively couple the first impurity regions to corresponding upper electrodes of the first and second capacitors; and

forming first and second bitlines across the first and second split wordlines, wherein the first and second bitlines are respectively coupled to the second impurity regions.

29. (New) The method of claim 28, wherein the capacitors are ferroelectric capacitors.

30. (New) The method of claim 29, wherein the forming first and second ferroelectric capacitors comprises:

forming a first electrode of the first ferroelectric capacitor over the second split wordline and forming a first electrode of the second ferroelectric capacitor over the first split wordline;

forming first and second ferroelectric layers respectively over surfaces of the first electrodes of the first and second ferroelectric capacitors; and

forming second electrodes of the first and second ferroelectric capacitors respectively over surfaces of the first and second ferroelectric layers.

31. (New) The method of claim 30, wherein forming the second electrodes of the first and second ferroelectric capacitors comprises:

forming a second electrode material layer of the ferroelectric capacitor on an entire surface including the first and second ferroelectric layers; and

selectively removing the second electrode material layer, wherein the second electrode of the first ferroelectric capacitor and the second electrode of the second ferroelectric capacitor are respectively formed on field regions at both sides of corresponding active regions.

32. (New) The method of claim 30, wherein forming the second electrodes of the first and second ferroelectric capacitors comprises:

forming a second electrode material layer of the ferroelectric capacitors on an entire surface including the first and second ferroelectric layers; and

selectively removing the second electrode material layer to form the second electrode of the first ferroelectric capacitor and the second electrode of the second ferroelectric capacitor, wherein the second electrodes are symmetrically formed in parallel to each other along the first and second split wordlines.

33. (New) The method of claim 32, wherein the second electrode of the first ferroelectric capacitor is formed from a region between source and drain regions of a second active region to a field region below a first active region, and wherein the second electrode of the second ferroelectric capacitor is formed from a region between source and drain regions of the first active region to a field region on the second active region.

34. (New) The method of claim 28, wherein the first and second impurity regions are respectively source regions and drain regions, wherein forming the first and second conductive layers comprises forming second plugs coupled to the first and second source regions through second contact holes.

35. (New) The method of claim 34, wherein the capacitors are ferroelectric capacitors, wherein forming the first and second conductive layer comprises forming first plugs coupled to the first and second drain regions through first contact holes, and wherein forming the first and second conductive layers comprises:

forming a conductive material layer on the entire surface including the second electrodes of the first and second capacitors; and

selectively removing the conductive material layer to form the first and second conductive layers, wherein the first conductive layer is directly coupled with the second electrode of the first capacitor and the second plug that is coupled to the first source region, and wherein the second conductive layer is directly coupled with the second electrode of the second capacitor and the second plug that is coupled to the second source region.

36. (New) The method of claim 35, comprising:

forming third plugs respectively coupled to the first plugs before forming the first and second bitlines, wherein the first bitline is coupled with the third plug coupled to the first drain region through the first plug, and wherein the second bitline is coupled with the third plug coupled to the second drain region through the first plug; and

forming a barrier metal layer after forming the first and second plugs.

37. (New) The method of claim 28, wherein the first electrode of the first capacitor is formed over the second split wordline and an insulating layer is formed therebetween, and wherein the first electrode of the second capacitor is formed over the first split wordline and an insulating layer is formed therebetween.

38. (New) The method of claim 28, further comprising electrically coupling the first split wordline with a first electrode of the second capacitor, and electrically coupling the second split wordline with a first electrode of the first capacitor.

39. (New) The method of claim 28, comprising:

forming a cell array having a matrix form of split wordline pairs crossing bitlines;

forming a wordline driver coupled to the wordlines;

forming a decoder coupled to the bitlines; and

forming an output unit coupled to the bitlines, wherein corresponding first and second split wordlines form split wordline pairs.

40. (New) A method for fabricating a device, the method comprising:

defining a first active region and a second active region on a semiconductor substrate;

forming first split wordline across the first active region and a second split wordline across the second active region;

forming first and second source and drain regions in the first and second active regions, respectively, wherein the source and drain regions are at opposite sides of the first and second split wordlines;

forming first plugs coupled to the first and second drain regions through a contact hole;

forming second plugs coupled to the first and second source regions through the contract hole;

respectively forming first electrodes of first and second capacitors over the second and first split wordlines;

forming insulating material layers on the first electrodes;

respectively forming island shaped second electrodes of the first and second capacitors on surfaces of the first and second insulating material layers;

respectively forming first and second conductive layers that couple the second plugs with the second electrodes of the first and second capacitors; and

forming first and second bitlines across the first and second split wordlines, wherein the first and second bitlines are coupled to the first and second drain regions through the first plugs.

41. (New) The method of claim 39, wherein the device is a nonvolatile ferroelectric memory device.